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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,996	03/12/2004	Chris E. Barns	10599-584002/P12765C	8779

20985 7590 10/17/2005

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EXAMINER	
VINH, LAN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,996	BARNS ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-17 and 19-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-9 and 15-17,19-22* is/are rejected.

7)☒ Claim(s) *10-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *31404*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 15-17, 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Boyd et al (US 2002/0028555)

Boyd discloses a method for fabrication a MOSFET. The method comprises the steps of:

forming a polysilicon feature on a semiconductor substrate having an intermediate gate dielectric layer 26 (col 3, paragraph 0059 ; fig. 1E)

depositing a first metal layer over the polysilicon feature; reacting the first metal layer with the polysilicon feature to form a metal silicide 36 (col 4, paragraph 0063)

depositing a dielectric layer 60 over the metal silicide and the semiconductor substrate (fig. 2C)

removing a portion of the dielectric layer over the metal silicide to expose a portion of the metal silicide 36 (col 4, paragraph 0072)

removing the portion of the metal silicide by chemical mechanical polishing (col 4, paragraph 0072)

removing the polysilicon feature 52 to create an opening in the gate dielectric layer (col 4, paragraph 0073; fig. 2E)

removing the gate dielectric laver (col 4, paragraph 0073; fig. 2E)

oxidizing the semiconductor substrate to form a new gate dielectric layer 62 (col 5, paragraph 0074)

Regarding claim 16, Boyd discloses the step of removing the dielectric by CMP (col 4, paragraph 0072)

Regarding claim 17, fig. 2D of Boyd discloses that the silicide layer 36 is polished by a faster polishing rate than the dielectric layer 60

Regarding claim 19, Boyd discloses filling the opening in the gate dielectric with metla layer 28 (col 5, paragraph 0077; fig. 2F)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-2, 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyd et al (US 2002/0028555) in view of Thomas et al (US 2002/0019202)

Boyd discloses a method for fabrication a MOSFET. The method comprises the steps of:

depositing a polysilicon layer 52 on the semiconductor substrate, removing a portion of the polysilicon laver to form a high region and a low region (fig. 2A)

forming a silicide layer 36 over the semiconductor substrate (col 4, paragraph 0070)

removing a portion of the silicide laver 36 at a first rate and to remove the polvsilicon laver at a second rate by CMP wherein the first rate is higher than the second rate (col 4, paragraph 0072, fig. 2D shows all of the silicide layer 36 is removed after the CMP process while portion of polysilicon layer 52 still remains

Unlike the instant claimed invention as per claim 1, Boyd fails to specifically disclose selecting chemical mechanical polishing parameters to remove the silicide layer at a higher rate than the polysilicon

Thomas, in a method for controlling of removal rate in CMP, discloses that the difference in removal rate is characterized by a parameter termed the selectivity ratio (col 1, paragraph 0005)

Since Boyd discloses removing a portion of the silicide laver 36 at a higher rate than polysilicon during the CMP process, one skilled in the art at the time the invention was

made would have found it obvious to modify Boyd CMP process by selecting chemical mechanical polishing parameters to remove the silicide layer at a higher rate than the polysilicon as per Thomas because Thomas discloses that it is desirable for the removal rate of each layer to differ significantly from each other in order to reduce planarality and maintain the integrity od the semiconductor substrate during polishing (col 1, paragraph 0005)

Regarding claim 2, fig. 2A shows that the high region and the low region are formed before the silicide layer is formed and the silicide layer is removed from the high region (fig. 2D)

Regarding claim 5, Boyd discloses forming a dielectric layer 60 over the silicide layer (col 4, paragraph 0071), removing a portion of the dielectric layer to expose the silicide layer (col 4, paragraph 0072)

Regarding claims 6-7, Boyd discloses that the dielectric layer 60 comprises silicon dioxide and other insulator (col 4, paragraph 0071)

Regarding claim 8, Boyd discloses removing the dielectric layer by CMP (col 4, paragraph 0072)

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boyd et al (US 2002/0028555) in view of Thomas et al (US 2002/0019202) and further in view of Buynoski (US 6,194,299)

Boyd as modified by Thomas has been described above. Unlike the instant claimed invention as per claim 9, Boyd and Thomas fails to disclose the step of forming a top

layer after forming the dielectric layer and removing a portion of the top layer before removing the portion of the dielectric layer

Buynoski discloses a method for fabricating of a low resistivity MOSFET comprises the step of forming a top layer 205 after forming the dielectric layer 204 and removing a portion of the top layer before removing the portion of the dielectric layer (col 3, lines 50-53; fig. 3)

One skilled in the art at the time the invention was made would have found it obvious to modify Boyd and Thomas by adding the step of forming a top layer after forming the dielectric layer and removing a portion of the top layer before removing the portion of the dielectric layer in order to form a mask to etch/remove the dielectric layer as taught by Buynoski (col 3, lines 53-55)

6. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyd et al (US 2002/0028555) in view of Thomas et al (US 2002/0019202)

Boyd discloses a method for fabrication a MOSFET. The method comprises the steps of:

depositing a polysilicon layer/material 52 on the semiconductor substrate, removing/patterning the polysilicon laver to form a high region and a low region (fig. 2A)

forming a silicide layer 36 in the high and low region (col 4, paragraph 0070, fig. 2B)

removing a portion of the silicide laver 36 from the high region at a first rate and to remove the polvsilicon laver at a second rate by CMP wherein the first rate is higher than the second rate (col 4, paragraph 0072, fig. 2D shows all of the silicide layer 36 in

the high region is removed after the CMP process while portion of polysilicon layer 52 still remains

Unlike the instant claimed invention as per claim 20, Boyd fails to specifically disclose selecting chemical mechanical polishing parameters to remove the silicide layer at a higher rate than the polysilicon

Since Boyd discloses removing a portion of the silicide laver 36 at a higher rate than polysilicon during the CMP process, one skilled in the art at the time the invention was made would have found it obvious to modify Boyd CMP process by selecting chemical mechanical polishing parameters to remove the silicide layer at a higher rate than the polysilicon as per Thomas because Thomas discloses that it is desirable for the removal rate of each layer to differ significantly from each other in order to reduce planarality and maintain the integrity od the semiconductor substrate during polishing (col 1, paragraph 0005)

Regarding claim 21, fig. 2A of Boyd shows the high region comprises polysilicon layer 56

Regarding claim 22, fig. 2D of Boyd shows all of the silicide layer 36 in the high region is removed after the CMP process while portion of polysilicon layer/feature 52 still remains

Allowable Subject Matter

6. Claims 10-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 10, the cited prior art of record fails to disclose a method for fabricating a semiconductor structure comprises the step of forming a top layer comprises TiN after forming the dielectric layer, in combination with the rest of the limitations of claim 10. The closest cited prior art of Buynoski (US 6,194,299) discloses a method for fabricating of a low resistivity MOSFET comprises the step of forming a top layer 205 of photoresist after forming the dielectric layer 204 and removing a portion of the top layer before removing the portion of the dielectric layer (col 3, lines 50-53; fig. 3)

Response to Arguments

7. Applicant's arguments, filed on 3/12/2004 with respect to claims 1-2, 5-9, 19-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LV
October 12; 2005